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09/811,456	03/20/2001	Masahito Isoda	108075-00056	2125

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-37* is/are allowed.

6)☒ Claim(s) *19,38 and 43-47* is/are rejected.

7)☒ Claim(s) *20,21 and 39-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 March 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/479,927* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. The request for a continued prosecution application (CPA) under 37 CFR 1.53(d) filed on 9/3/02 is acknowledged. 37 CFR 1.53(d)(1) was amended to provide that the prior application of a CPA must be: (1) a utility or plant application that was filed under 35 U.S.C. 111(a) before May 29, 2000, (2) a design application, or (3) the national stage of an international application that was filed under 35 U.S.C. 363 before May 29, 2000. *See Changes to Application Examination and Provisional Application Practice*, interim rule, 65 *Fed. Reg.* 14865, 14872 (Mar. 20, 2000), 1233 *Off. Gaz. Pat. Office* 47, 52 (Apr. 11, 2000). Since a CPA of this application is not permitted under 37 CFR 1.53(d)(1), the improper request for a CPA is being treated as a request for continued examination of this application under 37 CFR 1.114. *See id.* at 14866, 1233 *Off. Gaz. Pat. Office* at 48.

Response to Amendment

2. The amendment file on 9/3/02 has been received and entered in the case.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 19, 38, and 43-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (USP 5,789,948).

With respect to claim 19, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which are connected to p-channel transistors P1-P7 in Figure 1) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal which connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit (N1-N3, P1-P2), for receiving the amplified signal (the signal connected to gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply (power supply line which connected to p-channel transistors P1-P7 in Figure 1) and second power supply (ground), for receiving the first input signal (RDB); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1) for selectively enabling one of the differential amplifier circuit (N1-N3, P1-P2) and the second circuit (N4-N6, P3-P4) in accordance with a control signal (SAE, i.e., when signal SAE having logic HI, transistors N3 and N6 are turned on which enabling the differential amplifier circuit and the second circuit. Note that when both the differential amplifier and the second circuit are enabling, it meets the claim limitation "enabling one of the differential amplifier circuit and the second circuit" because the claim does not specifically recites that enabling one of the differential amplifier circuit and the second circuit while the other one is disabling at the same time), wherein the control circuit isolates a disabled one of the differential amplifier circuit (N1-N3, P1-P2) and the second circuit (N4-N6, P3-P4) from at least one of the first power supply and the second power supply (when signal SAE having logic LO, transistors N3 and N6 are turned

off which isolates the differential amplifier circuit and the second circuit from ground. Note that when both differential amplifier circuit and second circuits are disabling, it meets the claim limitation "isolates a disabled one of the differential amplifier circuit and second circuit" because the claim does not specifically recites that disabling one of the differential amplifier and the second circuit while enabling the other one at the same time).

With respect to claim 38, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2) for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), disposed between the first power supply (power supply line which connected to the p-channel transistors P1-P7) and the second power supply (ground), for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal (SAE, i.e., when signal SAE having logic HI, transistors N3, N6, and N7 are turned on which enabling the differential amplifier circuit and one of the first and second circuits. Note that when both first and second circuits are enabling, it meets the claim limitation "one of the first and second circuits" because the claim does not specifically recites that enabling one of the first and second circuits while disabling the other one

at the same time), wherein the control circuit isolates one of the first circuit and the second circuit in accordance with a control signal (SAE), wherein the control circuit isolates a disabled one of the first circuit and the second circuit from the first power supply and the second power supply (when signal SAE having logic LO, transistors N6 and N7 are turned off which isolates the first circuit and the second circuit from ground. Note that when both first and second circuits are disabling, it meets the claim limitation "isolates a disabled one of the first and second circuits" because the claim does not specifically recites that disabling one of the first and second circuits while enabling the other one at the same time).

With respect to claim 43, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which connected to the p-channel transistors P1-P7 in Figure 7) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit, for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB) and generating an output signal to the first circuit (the signal connected to the gate of transistor N9); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal (SAE, i.e.,

when signal SAE having logic HI, transistors N3 and N6 are turned on which enabling the differential amplifier circuit and the second circuit. Note that when both the differential amplifier and the second circuit are enabling, it meets the claim limitation "one of" because the claim does not specificity recites that selectively enabling one of the differential amplifier and the first circuit while disabling the other one at the same time).

With respect to claim 44, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which connected to the p-channel transistors P1-P7 in Figure 7) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit, for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB) and generating an output signal to the first circuit (the signal connected to the gate of transistor N9); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively isolating one of the differential amplifier circuit and the second circuit in accordance with a control signal (SAE, i.e., when signal SAE having logic LO, transistors N3 and N6 are turned off which isolating the differential amplifier circuit and the second circuit from ground. Note that when both the differential amplifier and the first circuit are disabling, it meets the claim limitation "one of"

because the claim does not specificity recites that isolating one of the differential amplifier and the second circuit while the other one is enabled at the same time).

With respect to claim 45, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which connected to the p-channel transistors P1-P7 in Figure 7) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit, for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB) and generating an output signal to the first circuit (the signal connected to the gate of transistor N9); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively isolating one of the differential amplifier circuit and the second circuit in accordance with a control signal (SAE, i.e., when signal SAE having logic LO, transistors N3 and N6 are turned off which isolating the differential amplifier circuit and the second circuit from ground. Note that when both the differential amplifier and the first circuit are disabling, it meets the claim limitation "one of" because the claim does not specifically recites that isolating one of the differential amplifier and the second circuit while enabling the other one at the same time), wherein the control circuit isolates a disabled one of the differential amplifier circuit and the second circuit from at least one

of the first power supply and the second power supply (when signal SAE having logic LO, transistors N3 and N6 are turned off which isolating the differential amplifier circuit and the second circuit from ground).

With respect to claim 46, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which connected to the p-channel transistors P1-P7 in Figure 7) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit, for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB) and generating a single output signal to the first circuit (the signal connected to the gate of transistor N9); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal (SAE, i.e., when signal SAE having logic HI, transistors N3 and N6 are turned on which enabling the differential amplifier circuit and the second circuit. Note that when both the differential amplifier and the first circuit are enabling, it meets the claim limitation "one of" because the claim does not specifically recites that enabling one of the differential amplifier and the second circuit while disabling the other one at the same time).

With respect to claim 47, Figure 1 of the Kim et al. reference disclose a circuit which includes: a differential amplifier circuit (N1-N3, P1-P2), disposed between a first power supply (power supply line which connected to the p-channel transistors P1-P7 in Figure 7) and a second power supply (ground), for receiving first and second input signals (RDB, RDBB) and generating an amplifier signal (the signal connected to the gate of transistor N8) corresponding to a voltage difference between the first and second input signals (RDB, RDBB); a first circuit (N7-N9, P5-P7, and the inverter), coupled to the differential amplifier circuit, for receiving the amplified signal (the signal connected to the gate of transistor N8) from the differential amplifier circuit (N1-N3, P1-P2); a second circuit (N4-N6, P3-P4), disposed between the first power supply and second power supply, for receiving the first input signal (RDB) and generating a single output signal to the first circuit (the signal connected to the gate of transistor N9); and a control circuit (whichever circuit that is used to generated signal SAE in Figure 1), coupled to the differential amplifier circuit and the first and second circuits, for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply (when signal SAE having logic LO, transistors N3 and N6 are turned off which isolating the differential amplifier circuit and the second circuit from ground. Note that when both the differential amplifier and the first circuit are disabling, it meets the claim limitation "one of" because the claim does not specifically recites that isolating one of the differential amplifier and the second circuit while enabling the other one at the same time).

Response to Arguments

5. Applicant's arguments filed on 9/3/02 have been considered but are moot in view of the new ground(s) of rejection.

Also note that, applicant's argument "according to claims 19 and 38, only one of the differential amplifier circuit and the second circuit is enabled" on page 8 in the Remarks is not persuasive because the claims do not recite "only one of". Note that the claim recites "one of the differential amplifier circuit and the second circuit is enabled" so when both of the differential amplifier circuit and the second circuit are enabled, it still meets the claim limitation "one of" because the claim does not recite "only one of". Moreover, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Allowable Subject Matter

6. Claims 20, 21 and 39-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

These claims would be allowed for the same reasons as indicated in the last office action (mailed on 5/3/02).

7. Claims 22-37 are allowed.

These claims are allowed for the same reasons as indicated in the last office action (mailed on 5/3/02).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

November 27, 2002

Long Nguyen
Art Unit: 2816